WHAT IS CLAIMED IS:

1. A micro controller, comprising a CPU, performing processing in accordance with a program,

said micro controller further comprising:

a memory, storing: compressed codes, resulting from the conversion of program codes into variable length codes;

an address conversion information, specifying the head address of each group of grouped program codes; and

a compressed code type information, specifying, according to each group, the code length of each compressed code contained in each group; and

a compressed code processing part, specifying, from a code address output by the CPU, an address conversion information and compressed code type information to be referred, using the specified address conversion information and the compressed code type information to determine the corresponding compressed code address, and reading the corresponding compressed code.

2. The micro controller as set forth in Claim 1, wherein

the memory furthermore stores dictionary information for decompressing compressed codes into the original codes and

the compressed code processing part refers the dictionary information to decompress the compressed code, which has been read, into the original code.

3. The micro controller as set forth in Claim 1, wherein

said compressed code processing part stores information for identifying the area in said memory in which compressed codes are

stored, the area in said memory in which the address conversion information are stored, and the area in which the compressed code type information are stored.

4. The micro controller as set forth in Claim 3, wherein said memory stores said address conversion information in the order of blocks of program codes, and

to store said compressed code type information in the order of the program codes.

5. The micro controller as set forth in Claim 2, wherein said dictionary information are stored in areas that are divided according to the code lengths of the corresponding compressed codes, and in each area, said dictionary information are stored in the order of the codes of said corresponding compressed codes.

6. The micro controller as set forth in Claim 5, wherein said compressed code processing part specifies, from the compressed code type information, the area in which the dictionary information to be referred is stored, and, based on the compressed code, specifies the dictionary information to be referred that is contained in the specified area.

7. The micro controller as set forth in Claim 1, wherein said compressed code processing part reads, from said memory and prior to reading a compressed code, a compressed code set, having a predetermined size and containing the compressed code to be read,

said micro controller is equipped with areas, respectively

storing temporarily the address conversion information, the compressed code type information, and the compressed code set that were used just immediately before,

to use the address conversion information and the compressed code type information that are stored temporarily in said areas in a case where the code address output by the CPU is contained in the same block as the compressed code that was read just immediately before, and

to read the compressed code from the compressed code set that is stored temporarily in said area in a case where the compressed code corresponding to the code address output by the CPU is contained in the compressed code set that was read just immediately before.

8. The micro controller as set forth in Claim 1, wherein said compressed code contains the same code as the original code.